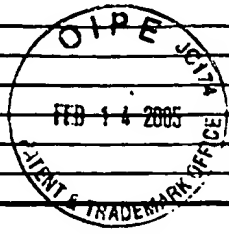


IDS Form PTO/SB/08: Substitute for form 1449A/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Application Number	09/487,483
		Filing Date	January 19, 2000
		First Named Inventor	Masue SHIBA
		Art Unit	2134
		Examiner Name	M. Simitoski
Sheet	1	of	1
		Attorney Docket Number	04329.2217



U.S. PATENTS AND PUBLISHED U.S. PATENT APPLICATIONS					
Examiner Initials	Cite No.	Document Number	Issue or Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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Note: Copies of the U.S. Patent Documents are not Required in IDS filed after October 21, 2004

FOREIGN PATENT DOCUMENTS						
Examiner Initials	Cite No.	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	Translation ⁶
		Country Code ³ Number ⁴ Kind Code ⁵ (if known)				
<i>MS</i>		DE-196 44 688 A1	04-30-1998			

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	Translation ⁶
<i>MS</i>		W. Drescher et al., VLSI Architectures for Multiplication in GF(2 ^m) for Application Tailored Digital Signal Processors, VLSI Signal Processing, IX, 1996., WORKSHOP ON SAN FRANCISCO, CA, USA 10/30 - 11/1/1996. ISBN: 0-7803-3134-6.	
<i>MS</i>		Search Report issued by French Patent Office on 12-16-04 in French Application No. 0000680	

Examiner Signature	<i>M. Simitoski</i>	Date Considered	2/12/08
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